32Kx8 bit Low Power CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.7 um CMOS
- Organization : 32K x 8
- Power Supply Voltage : Single 5V +/- 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-DIP, 28-SOP, 28-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

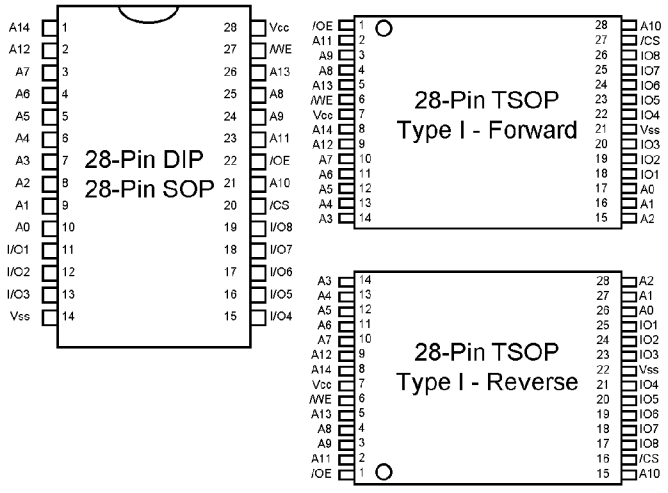
The KM62256C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

PRODUCT FAMILY

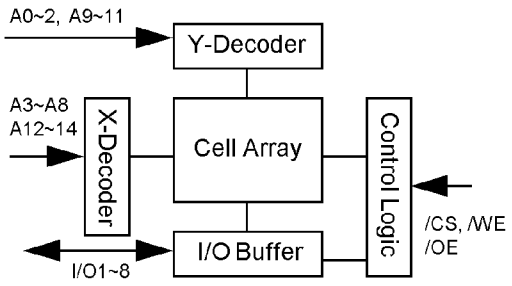
Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby(Isb1, Max)	Operating(Icc2)
KM62256CL	Commercial (0~70 °C)	45*/55/70ns	28-DIP, 28-SOP	100uA	70mA
KM62256CL-L			28-TSOP(I) R/F	20uA	
KM62256CLE	Extended (-25~-85 °C)	70/100ns	28-SOP	100uA	
KM62256CLE-L			28-TSOP(I) R/F	50uA	
KM62256CLI	Industrial (-40~85 °C)	70/100ns	28-SOP	100uA	
KM62256CLI-L			28-TSOP(I) R/F	50uA	

* measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



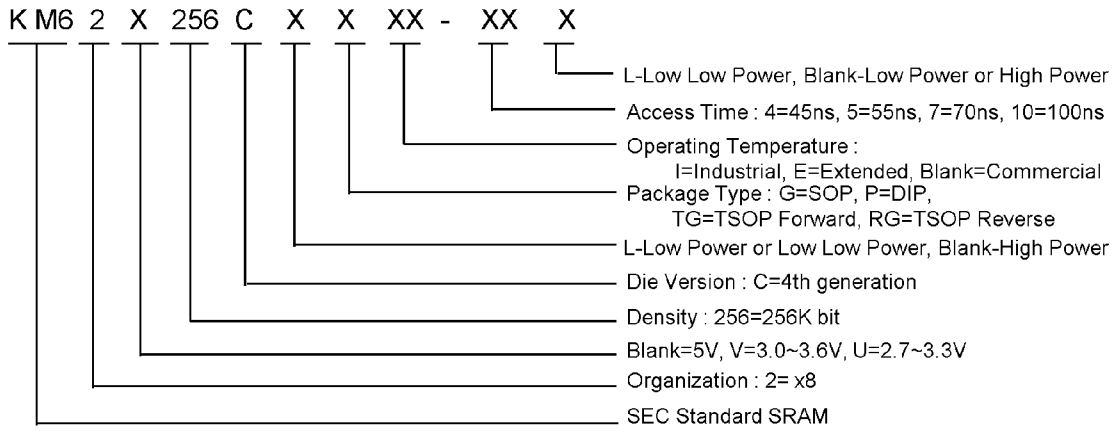
Pin Name	Function
A0~A14	Address Inputs
/WE	Write Enable Input
/CS	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power(5V)
Vss	Ground

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM62256CLP-4	28-DIP, 45ns, L-pwr	KM62256CLGE-7	28-SOP, 70ns, L-pwr	KM62256CLGI-7	28-SOP, 70ns, L-pwr
KM62256CLP-4L	28-DIP, 45ns, , LL-pwr	KM62256CLGE-7L	28-SOP, 70ns, LL-pwr	KM62256CLGI-7L	28-SOP, 70ns, LL-pwr
KM62256CLP-5	28-DIP, 55ns, , L-pwr	KM62256CLGE-10	28-SOP, 100ns, L-pwr	KM62256CLGI-10	28-SOP, 100ns, L-pwr
KM62256CLP-5L	28-DIP, 55ns, LL-pwr	KM62256CLGE-10L	28-SOP, 100ns, LL-pwr	KM62256CLGI-10L	28-SOP, 100ns, LL-pwr
KM62256CLP-7	28-DIP, 70ns, , L-pwr	KM62256CLTGE-7	28-TSOP F, 70ns, L-pwr	KM62256CLTGI-7	28-TSOP F, 70ns, L-pwr
KM62256CLP-7L	28-DIP, 70ns, LL-pwr	KM62256CLTGE-7L	28-TSOP F, 70ns, LL-pwr	KM62256CLTGI-7L	28-TSOP F, 70ns, LL-pwr
KM62256CLG-4	28-SOP, 45ns, L-pwr	KM62256CLTGE-10	28-TSOP F, 100ns, L-pwr	KM62256CLTGI-10	28-TSOP F, 100ns, L-pwr
KM62256CLG-4L	28-SOP, 45ns, LL-pwr	KM62256CLTGE-10L	28-TSOP F, 100ns, LL-pwr	KM62256CLTGI-10L	28-TSOP F, 100ns, LL-pwr
KM62256CLG-5	28-SOP, 55ns, L-pwr	KM62256CLRGE-7	28-TSOP R, 70ns, L-pwr	KM62256CLRGI-7	28-TSOP R, 70ns, L-pwr
KM62256CLG-5L	28-SOP, 55ns, LL-pwr	KM62256CLRGE-7L	28-TSOP R, 70ns, LL-pwr	KM62256CLRGI-7L	28-TSOP R, 70ns, LL-pwr
KM62256CLG-7	28-SOP, 70ns, L-pwr	KM62256CLRGE-10	28-TSOP R, 100ns, L-pwr	KM62256CLRGI-10	28-TSOP R, 100ns, L-pwr
KM62256CLG-7L	28-SOP, 70ns, LL-pwr	KM62256CLRGE-10L	28-TSOP R, 100ns, LL-pwr	KM62256CLRGI-10L	28-TSOP R, 100ns, LL-pwr
KM62256CLTG-4	28-TSOP F, 45ns, L-pwr				
KM62256CLTG-4L	28-TSOP F, 45ns, LL-pwr				
KM62256CLTG-5	28-TSOP F, 55ns, L-pwr				
KM62256CLTG-5L	28-TSOP F, 55ns, LL-pwr				
KM62256CLTG-7	28-TSOP F, 70ns, L-pwr				
KM62256CLTG-7L	28-TSOP F, 70ns, LL-pwr				
KM62256CLRG-4	28-TSOP R, 45ns, L-pwr				
KM62256CLRG-4L	28-TSOP R, 45ns, LL-pwr				
KM62256CLRG-5	28-TSOP R, 55ns, L-pwr				
KM62256CLRG-5L	28-TSOP R, 55ns, LL-pwr				
KM62256CLRG-7	28-TSOP R, 70ns, L-pwr				
KM62256CLRG-7L	28-TSOP R, 70ns, LL-pwr				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to 7.0	V	-
Power Dissipation	Pd	1.0	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM62256CL/L-L
		-25 to 85	°C	KM62256CLE/LE-L
		-40 to 85	°C	KM62256CLI/LI-L
Soldering temperature and time	Tsolder	260 °C , 10sec(Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.5	V
Input low voltage	Vil	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C , unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤50ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

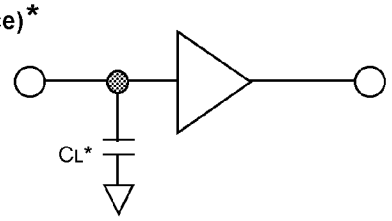
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or /WE=Vil Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS=Vil, Vin=Vih or Vil, Iio=0mA		-	7	15***	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS≤0.2V, Vil≤0.2V, Vin≥Vcc-0.2V, Iio=0mA		-	-	7****	mA
		Icc2	Min cycle, 100% duty /CS=Vil, Iio=0mA		-	-	70	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.4	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	1****	mA
Standby Current (CMOS)	KM62256CL	Isb1	/CS≥Vcc-0.2V Vin<0.2V or Vin>Vcc-0.2V	L(Low Power)	-	2	100	uA
	KM62256CL-I			LL(L Low Power)	-	1	20	uA
	KM62256CLE			L(Low Power)	-	-	100	uA
	KM62256CLE-L			LL(L Low Power)	-	-	50	uA
	KM62256CLI			L(Low Power)	-	-	100	uA
	KM62256CLI-L			LL(L Low Power)	-	-	50	uA

* 1) Commercial Product : Ta=0 to 70 °C , Vcc=5V+/-10%, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C , Vcc=5V+/-10%, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C , Vcc=5V+/-10%, unless otherwise specified
** Ta=25 °C
*** 20mA for Extended and Industrial Products
**** 10mA for Extended and Industrial Products
*****2mA for Extended and Industrial Products

A.C CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	



* Including scope and jig capacitance

* See test condition of DC and AC Operating characteristics
** Test load for 45ns Commercial Products

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62256CL/L-L	0~70 °C	5V +/- 10%	45*/55/70ns	Commercial
KM62256CLE/LE-L	-25~85 °C	5V +/- 10%	70/100ns	Extended
KM62256CLI/LI-L	-40~85 °C	5V +/- 10%	70/100ns	Industrial

* parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

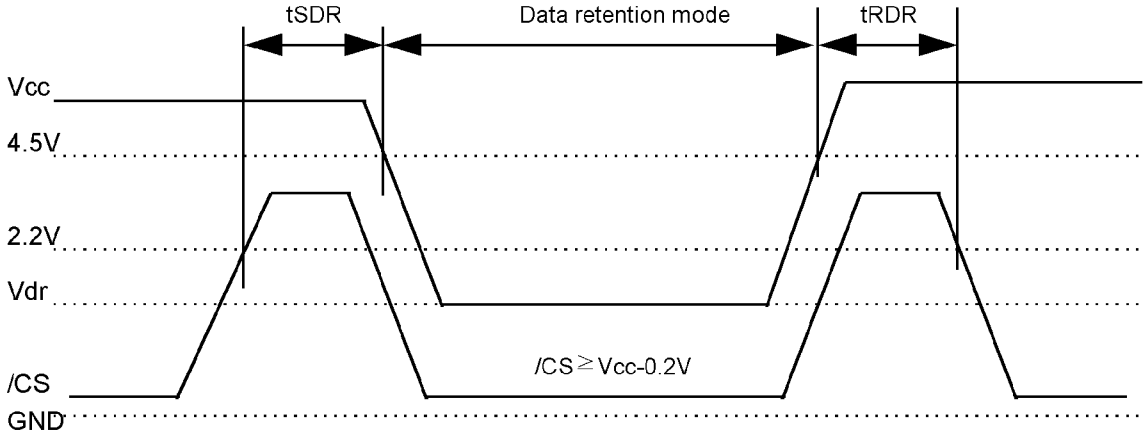
Parameter List		Symbol	Speed Bins								Units
			45ns		55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	30	0	35	ns
	Output disable to high-Z output	tOHZ	0	20	0	20	0	30	0	35	ns
	Output hold from address change	tOH	5	-	5	-	5	-	10	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	35	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	50	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	10	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	Idr	KM62256CL	Vcc=3.0V	L-Ver	-	1	50	uA
		KM62256CL-L	/CS ≥ Vcc-0.2V	LL-Ver	-	0.5	10	
		KM62256CLE		L-Ver	-	-	50	
		KM62256CLE-L		LL-Ver	-	-	25	
		KM62256CLI		L-Ver	-	-	50	
		KM62256CLI-L		LL-Ver	-	-	25	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

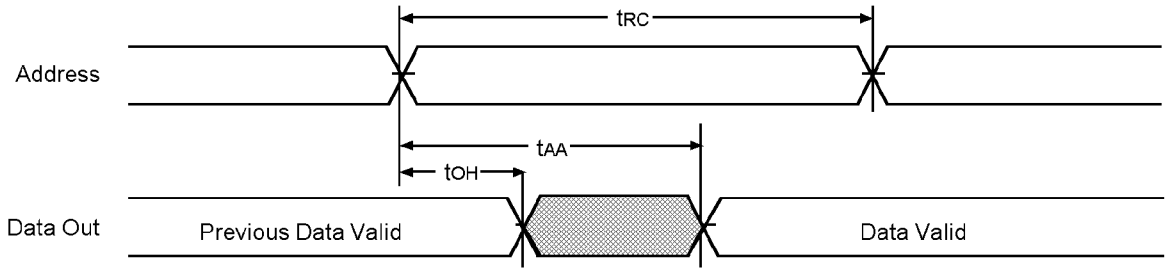
/CS	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

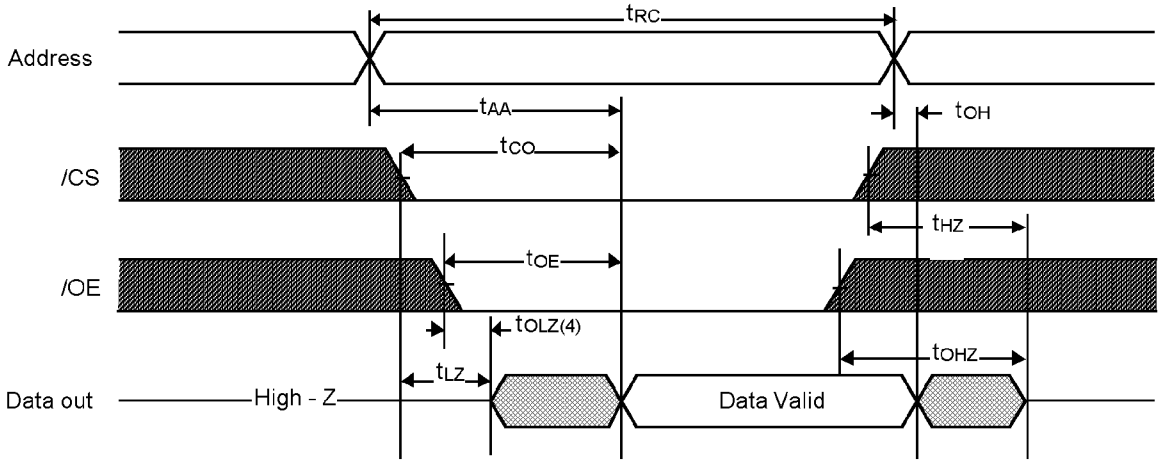
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih)



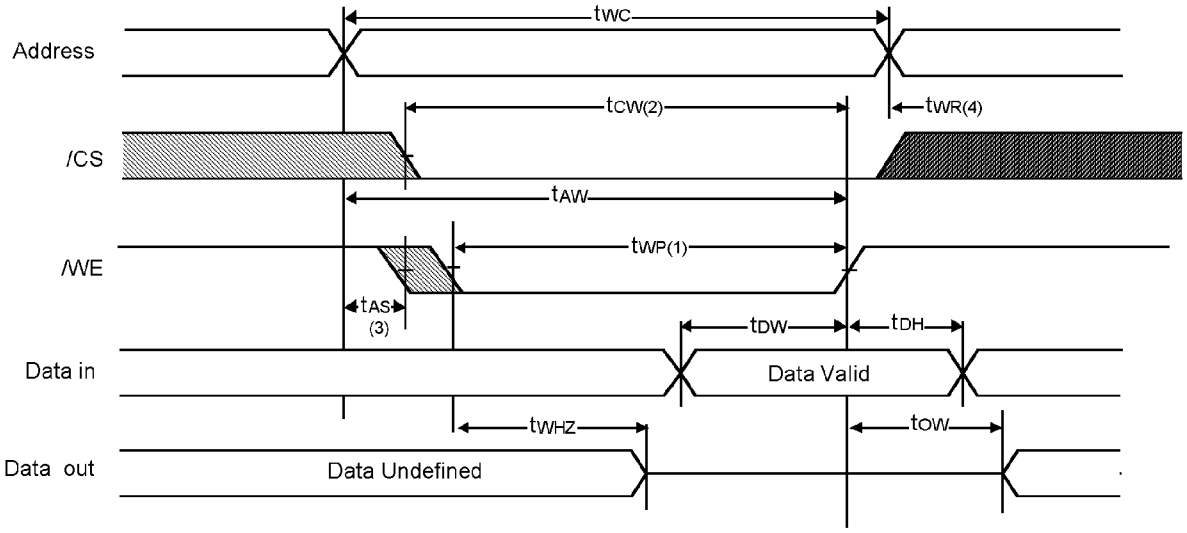
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



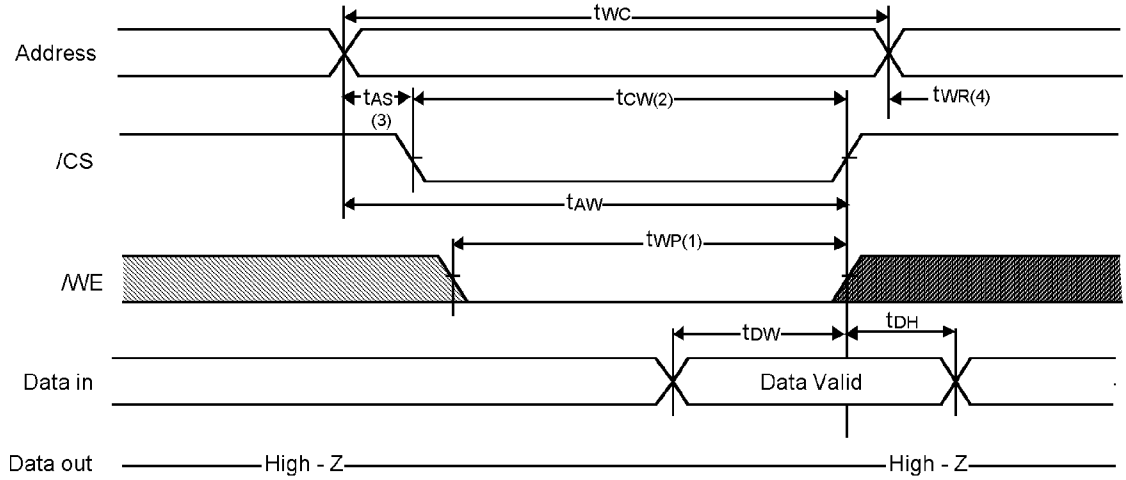
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.)both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



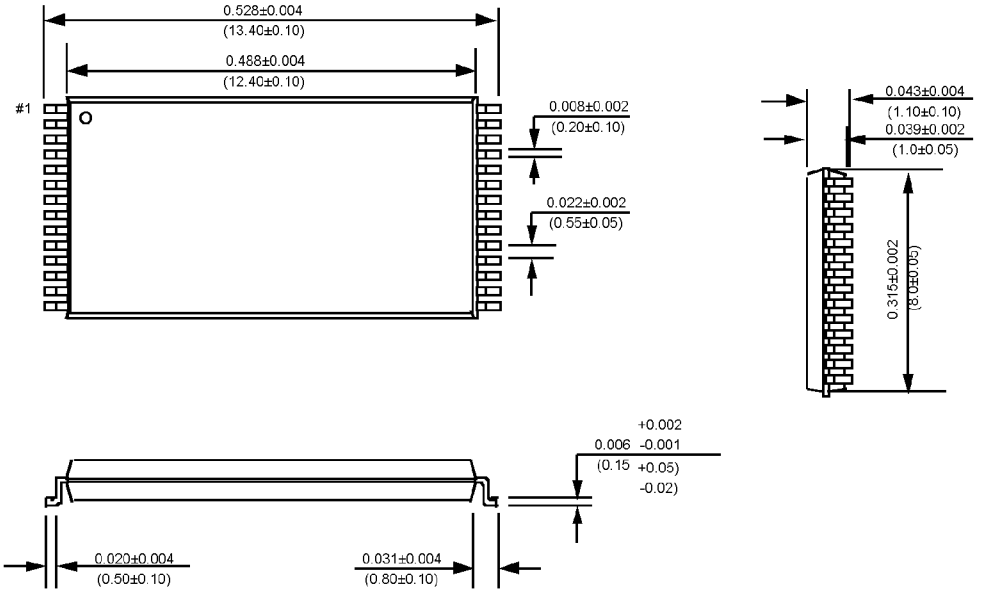
Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low : A write end at the earliest transition among /CS going high and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS, or /WE going high.

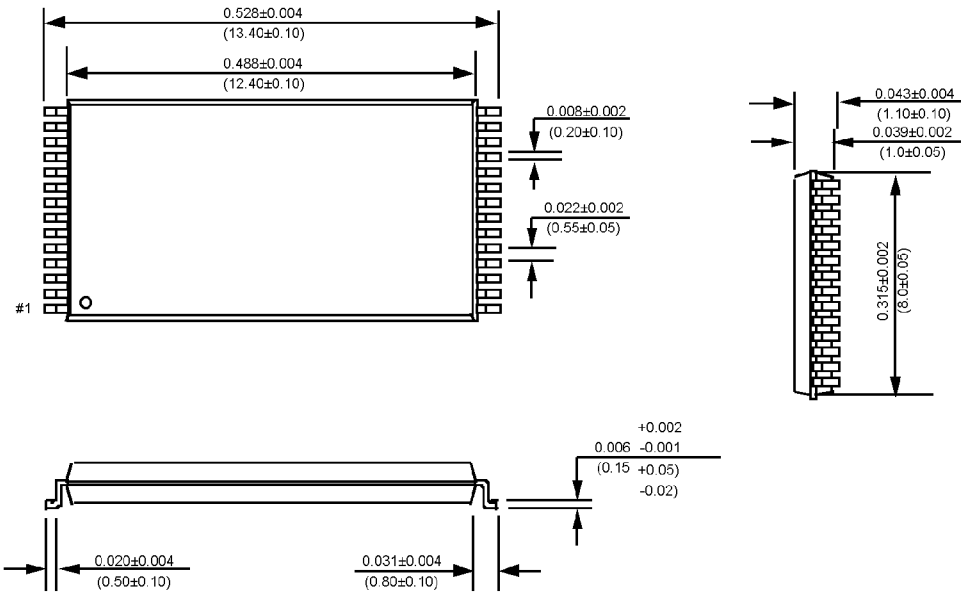
PACKAGE DIMENSION

28 PIN THIN SMALL OUTLINE PACKAGE (0813.4F)

Unit : Inches (Millimeters)

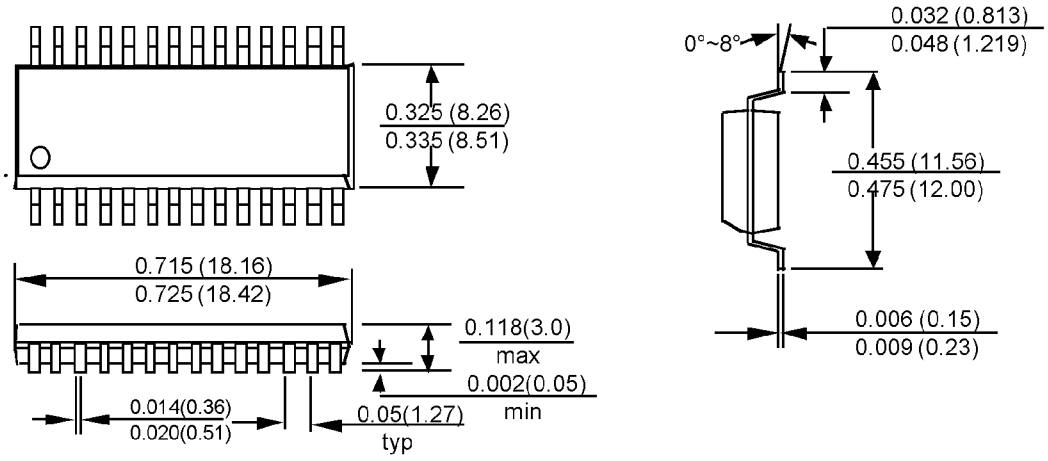


28 PIN THIN SMALL OUTLINE PACKAGE (0813.4R)

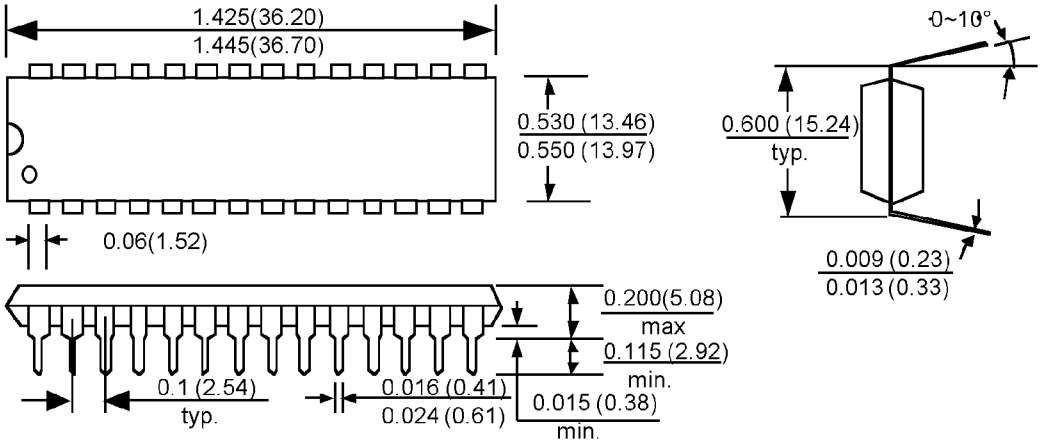


PACKAGE DIMENSION

28 PIN PLASTIC SMALL OUT LINE PACKAGE (450 mil) Unit : Inches (Millimeters)



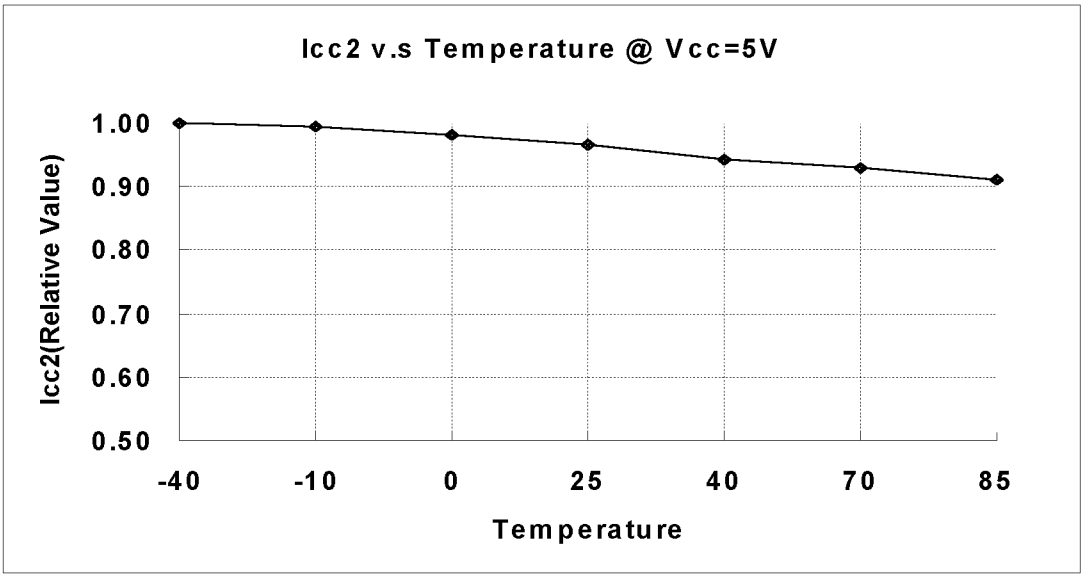
28 PIN PLASTIC DUAL IN LINE PACKAGE(600 mil)



TECHNICAL INFORMATION

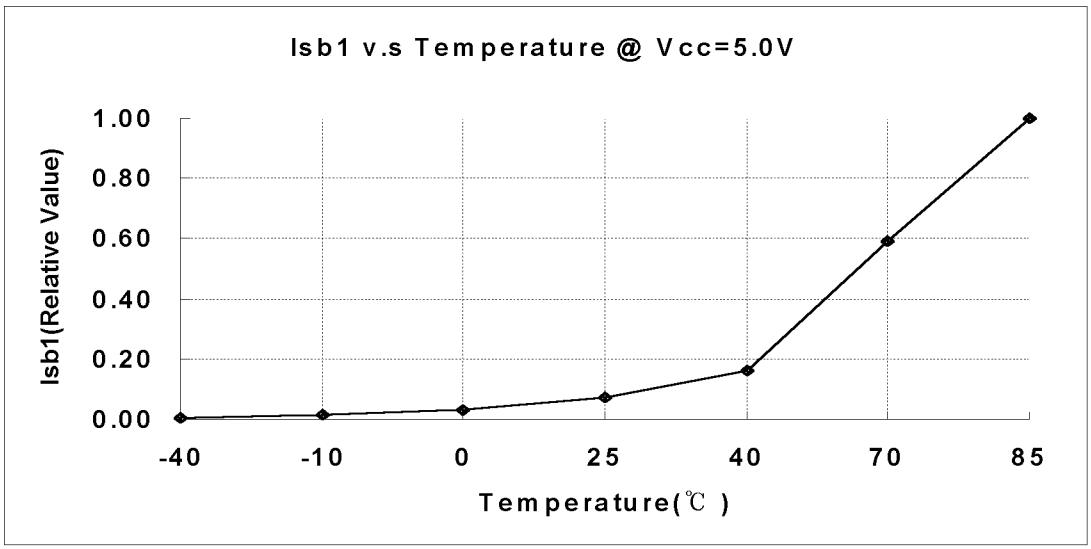
1) Icc2 characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and -40°C temperature. The basic relative value of Icc2 at that condition is set into 1.



2) Isb1(CMOS Level Standby Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 5.0V Vcc and 85°C temperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph is depicted by the relative value with the maximum value measured at Vdr=3.0V and 85°C temperature. The basic relative value of Idr at that condition is set into 1.